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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/532,514	03/21/2000	MAKOTO KUDO	105803	6717

25944 7590 06/13/2003

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
FERRIS III, FRED O	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/532,514	KUDO ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2123	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-28 have been presented for examination based on applicant's amendment filed on 3 March 2003. Claims 1-28 have been rejected by the examiner.

Response to Arguments

2. Applicant's arguments filed on 3 March 2003 (paper #9) have been fully considered.

Regarding applicant's response to IDS requirements: Applicants have provided a faxed copy of PTO-1449 received on 22 October 2002. Examiner agrees that applicants have cited the referenced prior art in the correct section of the PTO-1449. However, as noted during interview with applicant's representative on 26 March 2003 (see paper #11) applicants have not provided a copy of the referenced prior art to the PTO. Examiner will consider the cited reference once applicants have submitted a to the PTO.

Regarding applicant's response to Title objection: Applicants have amended the title. Examiner withdraws the objection to the title.

Regarding applicant's response to 35 U.S.C. 112(2) rejection: Applicants have argued that the 112(2) rejection is improper because the evidence that the scope of the claims is inconsistent with the specification cannot be derived form the specification (MPEP 2172). The examiner concurs that, in the case of the present invention, a 112(2) rejection is improper and therefore withdraws the 112(2) rejection of claims 1 and 19. However, the examiner reiterates that the subject matter which applicants

apparently regard as their invention, as it appears the specification on page 2, lines 3-10 and page 11, lines 11-27, ***is inconsistent with that which that is claimed****. In the specification and in the abstract, applicants' have stated that the invention relates to "the number of pins in the evaluation chip increasing in comparison to the number of terminal on the product chip" (see fig. 1a, b), and the difficulty in acquiring a package in which the evaluation chip can be mounted. This statement indicates that the invention is different from what is defined in the claims because, in the specification, and in the abstract, it appears that the applicant's invention is drawn to solving the problem of* ***"compatibility of terminals between the product and evaluation chips" and reduction of the number of terminals (pins) to achieve compatibility (page 2, line 9)****. Independent claims 1 and 19, however, only claim well-known features relating to a* ***microcomputer*** *for performing* ***information processing****, an* ***external bus*** *connectable to* ***emulation memory*** *and* ***external memory,*** *and* ***bus control*** *for connecting* ***processor to external bus.*** *These features can be found in nearly* ***any*** *microcomputer based emulation system.*

Regarding applicant's response to 35 U.S.C. 103(a) rejections: Applicants have argued that prior art does not disclose any type of microcomputer capable of switching to and from an emulation mode. The examiner asserts that, as cited in the previous office action, and in addition to being obvious and well-known in the art, this feature is clearly anticipated by Pawloski - U.S. 4,939,637 (see CL3-L62, Fig. 5-128, Fig. 6-128). Applicants have further argued that prior art does not teach a control signal for controlling an external memory connected to an external bus, and the second control

signal being different from the first control signal. The examiner again asserts that as cited in the previous office action, and in addition to being obvious and well-known in the art, this feature is clearly anticipated by Pawloski – U.S. 5,313,618 Fig. 2, 3, and Gephardt Fig. 2. The examiner further asserts that microprocessors including an external bus connected to an external memory having different control signals are very old and well-known in the art. (i.e. external bus and memory will include multiple (different) control signal such as those of Pawloski, Fig. Fig. 5D) (Also see Gephardt – U.S. 4,939,637 Fig. 2, 3, 7) Applicants have also argued that prior art does not teach a mode selection terminal selecting a forth mode for transmitting information from external memory to emulation memory after reset and emulation memory accessed by the processor. The examiner asserts that, as cited in the previous action, Pawloski discloses the use of modes of operation (i.e. emulation, etc., CL3-L62), additional modes are mere duplication and are commonly used in the art. In addition, transmitting information from external memory to emulation memory after reset and further having the emulation memory accessed by the processor is obvious since otherwise the invention would not operate. These techniques are also disclosed by Gephardt (CL2-L45-64) as previously cited. Accordingly, the examiner maintains the 103(a) rejections.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 19, and 20 are rejected under 35 U.S.C. 102(b) as being cl arly anticipated by U.S. Patent 6,240,377 issued to Kai et al.

Regarding claims 1, 19, and 20: Kai teaches a microcomputer based emulation system including a ***bus controller*** *having an* ***internal memory*** *that also accesses an* ***external bus,*** *which includes an* ***emulation memory,*** *and executes an* ***emulation mode****. (Abstract, Summary of Invention, CL3-L37-60, CL4-L4, 10-57, Figs. 1-3)*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. ***Claim 1, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,313,618 issued to Pawlowski in view of U.S. Patent 5,623,673 issued to Gephardt et al.***

Independent claims 1 and 20 are drawn to:
A ***microcomputer*** *for performing information processing and:*
A ***processor***
External bus *connectable to* ***emulation memory*** *and* ***external memory***

Bus control *for connecting* ***processor to external bus*** *(from internal memory to emulation memory) in* ***emulation mode***

Regarding independent claim 1 and 20: Claims 1 and 20 are claiming a microcomputer and bus control means that allows the processor to access an emulation memory and an external memory via an external bus that is switched from its internal memory via control signals. This technique is well known and in common use in the art. By way of example, Pawloski teaches a microcomputer (8051) having an ***internal memory*** *that also accesses an* ***external bus****, which includes an* ***emulation memory*** *and an external (RAM) memory. (Figs. 1, 2, CL1-L49) The microcomputer* ***controls*** *access the external bus by writing to* ***registers*** *(ports including dedicated* ***pins (terminals)****, CL10-L3) for selecting between memories and entering the* ***emulation mode****. (CL4-24) While Pawloski is in fact a dual processor system, the reference demonstrates the teachings of well known techniques where a microcomputer includes provisions for accessing emulation and external memory via an external bus. (Abstract, Summary of Invention, CL1-L49, CL10-L3, CL4-L24, CL4-L43-66 Figs. 1, 2, 5d)*

*Pawloski mentions, but does not explicitly teach the concept of running code (accessing) from different memories based on a selected "****mode****" after system reset.*

Gephardt teaches the concept of restricting local processor access to certain regions of memory via a "lock-out" register, and then running code in a predetermined portion of memory after system boot (reset). (CL2-L45-64) Gephardt teaches that in one lock-out mode (normal mode), the system will operate (i.e. access and run code) from a predetermined block of memory (as does the claimed invention when 2nd modes

is selected) following a system boot. (i.e. reset) When the lock-out register is set to the emulation mode, the system will run code (operate) from a different block (emulation code) of memory following ***system reset****. (Abstract, Summary of Invention, CL2-L45-64, CL8-L31-58, Fig. 2) In addition to being taught by Gephardt, the concept of a processor accessed register to control the selection of memory blocks is obvious and well known in the art. This concept is also taught by Pawloski as previously cited.*

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to modify the teachings of Pawloski relating to a microcomputer having an ***internal memory*** *that also accesses an* ***external bus****, which includes an* ***emulation memory*** *and an external (RAM) memory, with the teachings of Gephardt relating to restricting local processor access to certain regions of memory and then running (accessing) code in a predetermined portion of memory after system reset to realize the claimed invention. An obvious motivation exists since, as referenced by prior art, restricting processor access to a separate and independent memory (emulation) allows more efficient and timely program development and debugging.*

Regarding independent claim 19: Claim 19 merely claims the emulation method for the features of claim 1 and is therefore rejected using the same reasoning as previously cited above.

Claims 2-18, and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,939,637 issued to Pawlowski in view of of U.S. Patent 5,623,673 issued to Gephardt et al.

Dependent claims 2-9 are drawn to:
Mode** selection **terminal for emulation mode
***Mode selection register** (processor on/off control)*
*Processor **address bus connected to external address bus** (mode independent)*
*processor **data bus connected to external data bus** when emulation **mode on***
Control signal** for controlling **external memory** and second control signal for controlling **emulation memory
Second memory control includes second memory read active before first memory read
Mode selection to select which memory used after reset

*Regarding dependent claims 2-9: Pawloski teaches the use of a **"mode" selection register** that allows the processor to select emulation mode and further discloses a "pin" (terminal) where the signal is made available. (Fig. 5, 6, CL3-L61-66, CL10-L38-68) This implementation is commonly used in the art.*

*It would have been obvious to connect the processor **address bus connected directly to the external address bus** (claim 4) since the address lines are not bi-directional and, hence, need not be buffered, and the memory selection is performed independent of the address bus. The practice is also very common in the art since fewer (not needed) components are required.*

*It further have been obvious, and necessary, to have the processor **data bus connected to external data bus** when emulation **mode on**, since bi-directional data must flow between the processor and the emulation memory via the external data bus.*

It would also have been obvious, and necessary, to have the second memory read active control occur before first memory read since not doing so would result in a "collision" condition between read cycles of the memories.

*Pawloski does not explicitly teach the concept of running code (accessing) from different memories based on a selected "**mode**" after system reset.*

Gephardt teaches the concept of restricting local processor access to certain regions of memory via a "lock-out" register, and then running code in a predetermined portion of memory after system boot (reset). (CL2-L45-64) Gephardt teaches that in one lock-out mode (normal mode), the system will operate (i.e. access and run code) from a predetermined block of memory (as does the claimed invention when 2nd modes is selected) following a system boot. (i.e. reset) When the lock-out register is set to the emulation mode, the system will run code (operate) from a different block (emulation code) of memory following ***system reset****. (Abstract, Summary of Invention, CL2-L45-64, CL8-L31-58, Fig. 2) In addition to being taught by Gephardt, the concept of a processor accessed register to control the selection of memory blocks is obvious and well known in the art.*

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to modify the teachings of Pawloski relating to the use of a ***"mode" selection register*** *that allows the processor to select emulation mode, with the teachings of Gephardt relating to restricting local processor access to certain regions of memory and then running (accessing) code in a predetermined portion of memory* ***after system reset*** *to realize the claimed invention. An obvious motivation exists since, as referenced by prior art, restricting processor access to a separate and independent memory (emulation) allows more efficient and timely program development and debugging.*

Regarding dependent claims 10-18: Claims 10-18 merely claim the electronic equipment input source and output device for the features of claims 1-9 and are therefore rejected using the same reasoning as previously cited above.

The use of Internal and external microprocessor busses and a processor controlled means of selecting memory is obvious and well known and common to many modern microprocessor based system as is demonstrated by prior art.

Regarding new claims 20-28: Claim 20 is drawn the same well-known microprocessor/emulator limitations of claim 1 and is rejected using the same reasoning as previously cited above. Per claims 21-28, switching the emulation mode on and off would be obvious and necessary in order for the claimed invention to operate and is disclosed in the prior art as cited above. These features are also clearly anticipated by the prior art in Pawloski Figs. 2, 3 and Gephardt Fig. 2.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U. S. Patent 6,240,377 issued to Kai et al teaches external bus and emulation memory.

U.S. Patent 5,781,750 issued to Blomgren et al teaches emulation mode and register control.

U.S. Patent 5,062,034 issued to Bakker teaches multiple microcontroller bond-out.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

The Official Fax Numbers are:

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Fred Ferris. Patent Examiner

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May 8, 2003

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